CLAIMS

1. A method of forming a semiconductor construction, comprising:

forming a mass over a semiconductor substrate;

forming first and second layers over the mass, and over a region of the substrate proximate the mass;

removing the first and second layers from over the mass while leaving portions of the first and second layers over the region proximate the mass;

etching the first layer with an etch selective for the first layer relative to the second layer to remove at least some of the first layer from under the second layer and thereby form a channel over the region proximate the mass; and

forming a material within the channel.

2. The method of claim 1 wherein the mass comprises a memory bit which includes a first magnetic layer, a second magnetic layer, and a non-magnetic layer between the first and second magnetic layers.

3. The method of claim 1 wherein the removing the first and second layers from over the mass comprises chemical-mechanical polishing of the first and second layers.

4. The method of claim 1 wherein the first layer comprises silicon dioxide and the second layer comprises silicon nitride.

5. The method of claim 1 wherein the first layer comprises silicon nitride and the second layer comprises silicon dioxide.

6. The method of claim 1 wherein the second layer comprises silicon carbide and the first layer does not comprise silicon carbide.

7. The method of claim 1 wherein the second layer consists essentially of one or both of silicon and carbon; and wherein the first layer consists essentially of silicon and one or both of nitrogen and oxygen.

8. The method of claim 1, wherein the second layer consists essentially of silicon and one or both of nitrogen and oxygen; and wherein the first layer comprises carbon.

9. The method of claim 1 wherein the material formed within the channel is a soft magnetic material comprising one or more of nickel, iron and copper.

10. The method of claim 1 wherein the material formed within the channel consists essentially of mu-metal.

11. A method of forming a semiconductor construction, comprising:

forming a block comprising at least one magnetic composition over a semiconductor substrate;

forming first, second and third layers over the block, and over a region of the substrate proximate the block;

removing the second and third layers from over the block while leaving portions of the second and third layers over the region proximate the block; at least some of the second layer being removed from under the third layer to leaving a channel over the region proximate the block; and

forming a magnetic material within the channel.

12. The method of claim 11 further comprising removing the first layer from over the block.

13. The method of claim 11 wherein the removing the second and third layers from over the block comprises chemical-mechanical polishing of the second and third layers.

14. The method of claim 11 wherein the removing the second and third layers from over the block comprises chemical-mechanical polishing of the second and third layers, and wherein the chemical-mechanical polishing also removes the first layer from over the block.

15. The method of claim 11 wherein the first and third layers are identical to one another in composition, and wherein the second layer is different in composition from the first and third layers.

16. The method of claim 11 wherein the third layer comprises silicon dioxide and the second layer comprises silicon nitride.

17. The method of claim 11 wherein the first and third layers comprise silicon dioxide and the second layer comprises silicon nitride.

18. The method of claim 11 wherein the third layer comprises silicon nitride and the second layer comprises silicon dioxide.

19. The method of claim 11 wherein the first and third layers comprise silicon nitride and the second layer comprises silicon dioxide.

20. The method of claim 11 wherein the first and third layers comprise silicon carbide and the second layer does not comprise silicon carbide.

21. The method of claim 11 wherein the first and third layers consist essentially of one or both of silicon and carbon; and wherein the second layer consists essentially of silicon and one or both of nitrogen and oxygen.

22. The method of claim 11 wherein the third layer consists essentially of silicon and one or both of nitrogen and oxygen; and wherein the second layer comprises carbon.

23. The method of claim 11 wherein the first and third layers consist essentially of silicon and one or both of nitrogen and oxygen; and wherein the second layer comprises carbon.

24. The method of claim 11 wherein the magnetic material formed within the channel comprises one or more of nickel, iron and copper.

25. The method of claim 11 wherein the magnetic material formed within the channel consists essentially of mu-metal.

26. A method of forming a magnetoresistive memory device, comprising:

forming a memory bit comprising a stack which includes a first magnetic mass, a second magnetic mass, and a non-magnetic mass between the first and second magnetic masses;

forming first, second and third layers over the memory bit, and over a region proximate the memory bit;

removing the second and third layers from over the memory bit, while leaving portions of the second and third layers over the region proximate the memory bit; at least some of the second layer being removed from under the third layer to leaving a channel over the region proximate the memory bit; and

forming a magnetic material within the channel.

27. The method of claim 26 further comprising removing the first layer from over the memory bit.

28. The method of claim 26 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers.

29. The method of claim 26 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers; and wherein the removal of at least some of the second layer from under the third layer occurs subsequent to the chemical-mechanical polishing and comprises an etch selective for the second layer relative to the third layer.

30. The method of claim 26 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers, and wherein the chemical-mechanical polishing also removes the first layer from over the memory bit.

31. The method of claim 26 wherein the first and third layers are identical to one another in composition, and wherein the second layer is different in composition from the first and third layers.

32. The method of claim 26 wherein the third layer comprises silicon dioxide and the second layer comprises silicon nitride.

33. The method of claim 26 wherein the first and third layers comprise silicon dioxide and the second layer comprises silicon nitride.

34. The method of claim 26 wherein the third layer comprises silicon nitride and the second layer comprises silicon dioxide.

35. The method of claim 26 wherein the first and third layers comprise silicon nitride and the second layer comprises silicon dioxide.

36. The method of claim 26 wherein the first and third layers comprise silicon carbide and the second layer does not comprise silicon carbide.

37. The method of claim 26 wherein the first and third layers consist essentially of one or both of silicon and carbon; and wherein the second layer consists essentially of silicon and oxygen.

38. The method of claim 37 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers; and wherein the removal of at least some of the second layer from under the third layer occurs subsequent to the chemical-mechanical polishing and comprises an etch selective for the second layer relative to the third layer, the etch utilizing one or both of ammonium fluoride and hydrofluoric acid.

39. The method of claim 26 wherein the third layer consists essentially of silicon and one or both of nitrogen and oxygen; and wherein the second layer comprises carbon.

40. The method of claim 26 wherein the first and third layers consist essentially of silicon and one or both of nitrogen and oxygen; and wherein the second layer comprises carbon.

41. The method of claim 40 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers; and wherein the removal of at least some of the second layer from under the third layer occurs subsequent to the chemical-mechanical polishing and comprises an etch selective for the second layer relative to the third layer, the etch utilizing an O_2 plasma.

42. The method of claim 26 wherein the magnetic material formed within the channel comprises one or more of nickel, iron and copper.

43. The method of claim 26 wherein the magnetic material formed within the channel consists essentially of mu-metal.

44. The method of claim 26 wherein the magnetic material consists essentially of nickel and iron.

45. The method of claim 26 wherein the magnetic material consists essentially of nickel and copper.

46. A method of forming a magnetoresistive memory device, comprising:

forming a memory bit comprising a stack which includes a first magnetic mass, a second magnetic mass, and a non-magnetic mass between the first and second magnetic masses;

forming first, second and third layers over the memory bit, and over a region proximate the memory bit;

removing the second and third layers from over the memory bit, while leaving portions of the second and third layers over the region proximate the memory bit;

etching the second layer with an etch selective for the second layer relative to the third layer to remove at least some of the second layer from under the third layer and thereby form a channel over the region proximate the memory bit;

forming a first material within the channel to only partially fill the channel; and

forming a second material within the partially-filled channel, the second material being a magnetic material.

47. The method of claim 46 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers.

48. The method of claim 46 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers; and wherein the removal of at least some of the second layer from under the third layer occurs subsequent to the chemical-mechanical polishing and comprises an etch selective for the second layer relative to the third layer.

49. The method of claim 46 wherein the removing the second and third layers from over the memory bit comprises chemical-mechanical polishing of the second and third layers, and wherein the chemical-mechanical polishing also removes the first layer from over the memory bit.

50. The method of claim 46 wherein the first and third layers are identical to one another in composition, and wherein the second layer is different in composition from the first and third layers.

51. The method of claim 46 wherein the first and third layers comprising electrically insulative materials, and wherein the second layer comprises a metal-containing material.

52. The method of claim 46 wherein:

the first and third layers comprising electrically insulative materials;

the second layer comprises a metal-containing material; and

the first material formed within the channel comprises a dielectric material.

53. The method of claim 52 wherein the dielectric material comprises silicon dioxide.

54. The method of claim 52 further comprising forming a conductive line over the memory bit, the conductive line being utilized to impart a magnetic field in the memory bit during writing of information to the memory bit; and wherein the conductive line electrically contacts the magnetic material that is formed within the channel.

55. A magnetoresistive memory construction, comprising:

a substrate;

a memory bit supported by the substrate and comprising a stack which includes a first magnetic mass, a second magnetic mass, and a non-magnetic mass between the first and second magnetic masses;

first, second and third layers over a region of the substrate proximate the memory bit, the second layer being recessed relative to the first and third layers to define a channel proximate the memory bit; and

a magnetic material within the channel.

56. The construction of claim 55 wherein the magnetic material within the channel comprises one or more of nickel, iron and copper.

57. The construction of claim 55 wherein the magnetic material within the channel consists essentially of mu-metal.

58. The construction of claim 55 wherein the magnetic material within the channel consists essentially of nickel and iron.

59. The construction of claim 55 wherein the magnetic material within the channel consists essentially of nickel and copper.

60. The construction of claim 55 wherein the memory bit has a lateral periphery defined thereby, and wherein the channel extends entirely around the lateral periphery of the memory bit.

61. The construction of claim 55 wherein the first and third layers are identical to one another in composition, and wherein the second layer is different in composition from the first and third layers.

62. The construction of claim 55 wherein the third layer comprises silicon dioxide and the second layer comprises silicon nitride.

63. The construction of claim 55 wherein the first and third layers comprise silicon dioxide and the second layer comprises silicon nitride.

64. The construction of claim 55 wherein the third layer comprises silicon nitride and the second layer comprises silicon dioxide.

65. The construction of claim 55 wherein the first and third layers comprise silicon nitride and the second layer comprises silicon dioxide.

66. The construction of claim 55 wherein the first and third layers comprise silicon carbide and the second layer does not comprise silicon carbide.

67. The construction of claim 55 wherein the first and third layers consist essentially of one or both of silicon and carbon; and wherein the second layer consists essentially of silicon and one or both of oxygen and nitrogen.

68. A magnetoresistive memory construction, comprising:

a substrate;

a memory bit supported by the substrate and comprising a stack which includes a first magnetic mass, a second magnetic mass, and a non-magnetic mass between the first and second magnetic masses;

first, second and third layers over a region of the substrate proximate the memory bit, the second layer being recessed relative to the first and third layers to define a channel proximate the memory bit;

a first material within the channel and only partially filling the channel; and

a second material within the partially-filled channel, the second material being different in composition from the first material and being a magnetic material.

69. The construction of claim 68 wherein the first material is a non-magnetic material.

70. The construction of claim 68 wherein the memory bit has a lateral periphery defined thereby, and wherein the channel extends entirely around the lateral periphery of the memory bit.

71. The construction of claim 68 wherein the magnetic material within the channel comprises one or more of nickel, iron and copper.

72. The construction of claim 68 wherein the magnetic material within the channel consists essentially of mu-metal.

73. The construction of claim 68 wherein the first and third layers are identical to one another in composition, and wherein the second layer is different in composition from the first and third layers.

74. The construction of claim 68 wherein the first and third layers comprising electrically insulative materials, and wherein the second layer comprises a metal-containing material.

75. The construction of claim 68 wherein the first and third layers comprising electrically insulative materials; wherein the second layer comprises a metal-containing material; and wherein the first material within the channel comprises a dielectric material.

76. The construction of claim 75 wherein the dielectric material comprises silicon dioxide.

77. The construction of claim 75 further comprising a conductive line over the memory bit, the conductive line being utilized to impart a magnetic field in the memory bit during writing of information to the memory bit; and the conductive line electrically contacting the magnetic material that is within the channel.